Silicon photonics MPW offering 2022

VTT's open access multi-project wafer runs for 3 µm silicon photonics platform

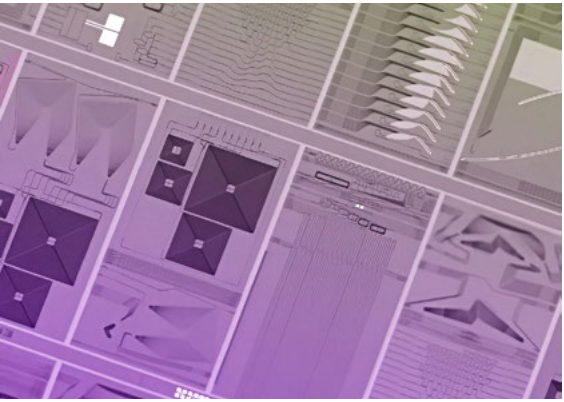
Runs are optimal for low-cost, low barrier prototyping and evaluation of photonic integrated circuits.

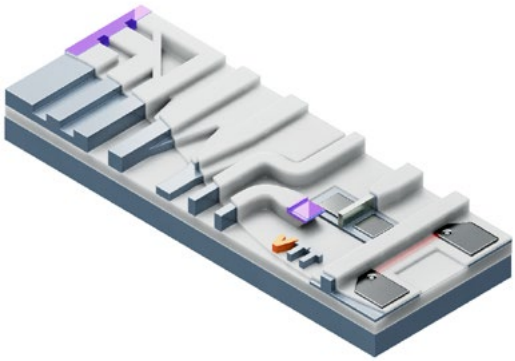
Design support

A process design kit (PDK) is offered to multi-project wafer run (MPW) participants to assist in the design work. The documentation describes the layout design guidelines and the design rules. VTT also offers layout design as an additional service.

Pricing model

Pricing is based on the choice of the design area size and the selected process flow. It includes the delivery of several identical chips and additional chips can be provided for additional cost as indicated in the pricing table.





Process flows

The process can be chosen from three alternatives: passive, active, and Ge-PD. Planarization (for routing electrical wires on the chip) and solder plating (for flip-chip integration of active components) are also available for extra cost.

Passive process flow includes the basic rib and strip silicon waveguide processing. Also provided are Al-coated facet reflectors for resonators and echelle gratings. For coupling, both etched waveguide facets and up-reflecting mirrors are available with AR-coating for 1310 nm or 1550 nm.

Active process flow includes the same process steps as the passive process flow but adds Al for electrical wiring and silicon implantation (p- and n-type) steps for thermo-optic and PIN phase shifters.

Ge-PD process flow extends the offering of the active process flow by providing also photodiodes. Separate designs are available for <1 GHz monitor and for fast photodiodes.

Deadlines

The MPW registration deadline is one month before the design deadline. In case a mask design is not delivered to VTT before the design deadline, there will be a one-time option to postpone the participation to the next suitable run for a small transfer fee.

How to join

You can express your interest in joining an MPW run by sending an email to **silicon.photonics@vtt.fi**. Access to the PDK documentation requires signing a design kit license agreement (DKLA) with VTT.

Design Area	Base Price (BP)			Delivered Chips	Chips for Additional 50% BP
	Passive	Active	Ge-PD		
5 × 4.75 mm^2	7.2 k€	11.3 k€	20.5 k€	5	+5
5 × 9.5 mm^2	11.3 k€	16.4 k€	35.8 k€	10	+10
20 × 19.5 mm^2	30.7 k€	46 k€	72.5 k€	3	+3

Design Deadline	Available process flows		
	Passive	Active	Ge-PD
4 April	x		
4 July	x	x	
3 October	x	x	x

For technical reference see

DOI 10.1109/ JSTQE.2019.2908551

Aalto et al.: “Open-Access 3-µm SOI Waveguide Platform for Dense Photonic Integrated Circuits”

VTT

Get in touch with us:

Piia Konstari
Solution Sales Lead
+358 50 576 3706
piia.konstari@vtt.fi

Timo Aalto
Research Team Leader
+358 40 848 5037
timo.aalto@vtt.fi

silicon.photonics@vtt.fi
www.vtt.fi/siliconphotonics

vttresearch.com **beyond the obvious**